frequency identification (RFID), and the like or wired communications manners such as universal serial bus (USB), SATA, HSIC, SCSI, Firewire, peripheral component interconnection (PCI), PCI express (PCIe), nonvolatile memory express (NVMe), universal flash storage (UFS), secure digital (SD), SDIO, universal asynchronous receiver transmitter (UART), serial peripheral interface (SPI), high speed SPI (HS-SPI), RS232, inter-integrated circuit (I2C), HS-I2C, integrated-interchip sound (I2S), Sony/Philips digital interface (S/PDIF), multimedia card (MMC), embedded MMC (eMMC), and so on.

[0204] The user interface **1500** may communicate with a user under control of the processor **1100**. For example, the user interface **1500** may include user input interfaces such as a keyboard, a keypad, buttons, a touch panel, a touch screen, a touch pad, a touch ball, a camera, a microphone, a gyroscope sensor, and a vibration sensor. The user interface **150** may further include user output interfaces such as a liquid crystal display (LCD), an organic light-emitting diode (OLED) display device, an active matrix OLED (AMOLED) display device, a light-emitting diode (LED), a speaker, and a motor.

[0205] As described with reference to FIGS. **1** to **15**, when one or more of the driver circuits **13** to **16** described with reference to FIGS. **5** to **8** are applied to the storage device **1300**, the operating speed of the storage device **1300** may be improved, and the complexity and area thereof may be reduced. This may mean that the operating speed of the computing device **1000** is improved and the complexity and area thereof are reduced Furthermore, a manufacturing cost of the storage device **1300** and the computing device **1000** may be reduced.

[0206] According to example embodiments of inventive concepts, a driver circuit may be configured to drive a clamp transistor using an amplifier. Thus, a driving capacity of the driver circuit may be improved. Furthermore, the driver circuit may be composed of a single stage amplifier. Thus, the number of transistors constituting the driver circuit may be reduced, and thus the area of the driver circuit may be reduced.

[0207] FIG. **18** is a block diagram illustrating an embodiment including a plurality of driver circuits according to example embodiments of inventive concepts. Referring FIG. **18**, a load circuit LC may be connected with the first driver circuit **13** or **14** shown in FIGS. **5** and **6** and the second driver circuit **15** or **16** shown in FIGS. **7** and **8**. The load circuit LC may be supplied with a setting voltage VSET directly from an external power source (not shown) as shown in FIGS. **5** and **7** or supplied with the setting voltage VSET from the first and second driver circuits **14** and **16** as shown in FIGS. **6** and **8**. When the setting voltage VSET is supplied from the driver circuits **14** and **16**, the load circuit LC may be floated from the external power source or also receive the setting voltage VSET from the external power source. The driver circuit **13** or **14** may be used to decrease a voltage of the load circuit LC. The driver circuit **15** or **16** may be used to increase a voltage of the load circuit LC.

[0208] As shown in FIG. **18**, two or more driver circuits may be connected with a load circuit to drive a voltage of the load circuit. Driver circuits with the same type (e.g., increasing or decreasing type) may enhance driving capacity in parallel. Driver circuits with different types (e.g., increasing and decreasing types) may provide increasing capability and decreasing capability of the voltage of the load circuit. Types and a number of driver circuits connected to the load circuit is not limited.

[0209] Even though hardware implementations (e.g., specific circuits) of driver circuits according to example embodiments have been described with reference to FIGS. **3** and **5-8** of the present application, one of ordinary skill in the art would appreciate that a driver module could alternatively implement features of the above-described driver circuits. For example, a driver module may include a driver memory (e.g., memory device) and a controller (e.g., microprocessor) configured to execute computer-readable code (e.g., software) stored in the driver memory, wherein the computer-readable code transforms the controller into a special-purpose controller configured to perform some or all of the operations described herein as being performed by one or more of the driver circuits according to example embodiments in FIGS. **3** and **5-8** of the present application.

[0210] It should be understood that example embodiments described herein should be considered in a descriptive sense only and not for purposes of limitation. Descriptions of features or aspects within each device or method according to example embodiments should typically be considered as available for other similar features or aspects in other devices or methods according to example embodiments. While some example embodiments have been particularly shown and described, it will be understood by one of ordinary skill in the art that variations in form and detail may be made therein without departing from the spirit and scope of the claims.

1. A driver circuit, comprising:

a clamp transistor including a clamp gate, a first clamp node, and a second clamp node connected to a charge node;

a comparison voltage transistor including a comparison voltage gate configured to receive a reference voltage, a first comparison voltage node configured to receive a first voltage, and a second comparison voltage node configured to output a comparison voltage;

an amplification transistor including an amplification gate connected to the charge node, a first amplification node connected to the second comparison voltage node of the comparison voltage transistor and configured to receive the comparison voltage, and a second amplification node connected to the clamp gate of the clamp transistor;

a bias transistor including a bias gate configured to receive a bias voltage, a first bias node connected to the clamp gate of the clamp transistor, and a second bias node configured to receive a second voltage; and

a charge circuit, the charge circuit being one of configured to drain a current from the charge node through the clamp transistor and configured to supply a current to the charge node through the clamp transistor.

2. The driver circuit of claim **1**, wherein

the clamp transistor and the amplification transistor are PMOS transistors, and

the comparison voltage transistor and the bias transistor are NMOS transistors.

3. The driver circuit of claim **1**, wherein

the first voltage is a power supply voltage, and

the second voltage is a ground voltage.